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Presented for filing is a new original patent application of:

Applicant: TOSHIMITSU TANIGUCHI, TAKASHI ARAI AND MASASHIGE AOYAMA

Title: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THEREOF

Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

	Pages
Specification	22
Claims	9
Abstract	21
Declaration	4
Drawing(s)	14

Enclosures:

- Assignment cover sheet and an assignment, 4 pages, and a separate $40 fee.
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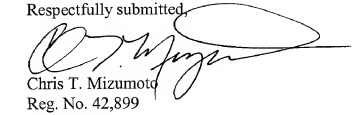

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APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THEREOF

APPLICANT: TOSHIMITSU TANIGUCHI, TAKASHI ARAI AND MASASHIGE AOYAMA

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SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device and its manufacturing method, further detailedly relates to technique for integrating various type of MOS transistors composing a driver for driving a liquid crystal for example on one semiconductor substrate.

2. Description of the Related Art

Referring to the drawings, a conventional type semiconductor device and its manufacturing method will be described below. The driver for driving a liquid crystal described above is composed of an N-channel MOS transistor and a P-channel MOS transistor which are respectively a logic device of 3 V for example, an N-channel MOS transistor and a P-channel MOS transistor respectively of 30 V for example which respectively have high resistance to voltage, an N-channel double-diffused (D) MOS transistor and a P-channel DMOS transistor and an N-channel MOS transistor of 30 V for example for a level shifter and others.

As for the DMOS transistor structure described above, impurities different in a conductive type are diffused into a diffused layer formed on the side of the main surface of a

semiconductor substrate so as to form a new diffused layer, difference in diffusion in the lateral direction of these diffused layers is utilized for effective channel length and a short channel is formed to be a device in which on-state resistance is reduced.

Fig. 12 is a sectional view for explaining a conventional type MOS transistor and shows the structure of an N-channel DMOS transistor as an example. The description of the structure of a P-channel MOS transistor is omitted, however, it is well-known that a P-channel MOS transistor is different only in a conductive type from an N-channel MOS transistor and has the similar structure.

As shown in Fig. 12, a reference numeral 51 denotes a semiconductor substrate of one conductive type, for example a P type, 52 denotes an N-type well, a P-type body layer 53 is formed in the N-type well 52, an N-type diffused layer 54 is formed in the P-type body layer 53 and an N-type diffused layer 55 is formed in the N-type well 52. A gate electrode 57 is formed on the surface of the substrate via a gate oxide film 56 and a channel layer 58 is formed in the superficial area of the P-type body layer 53 immediately under the gate electrode 57.

The N-type diffused layer 54 functions as a source diffused layer, the N-type diffused layer 55 functions as a drain diffused layer and the N-type well 52 under an oxide film

59 according to LOCOS method functions as a drift layer. Reference numerals 60 and 61 respectively denote a source electrode and a drain electrode, 62 denotes a P-type diffused layer for acquiring the electric potential of the P-type body layer 53 and 63 denotes a layer insulating film.

In the DMOS transistor described above, the concentration on the surface of the N-type well 52 is enhanced by diffusing impurities into it, as a result, current easily flows on the surface of the N-type well 52 and resistance to voltage can be enhanced.

The DMOS transistor having such structure is called surface relaxation-type ((REduced SURface Field: RESURF) DMOS and the concentration of dopants in the drift layer of the N-type well 52 is set so that it meets a condition of RESURF. Such technique is disclosed in JP-A-9-139438 and others.

In the DMOS transistor described above is formed, high temperature heat treatment for forming the P-type body layer 53 is required after a gate electrode is formed, therefore, as the concentration in a profile ruled every 0.35 μm for example in a microdevice operated at low voltage gets out of order, a micro MOS transistor starts to be formed in the present circumstances after a gate electrode of a DMOS transistor is formed and high temperature heat treatment for forming a P-type body layer is finished and there is a problem that a manufacturing process is extended.

As the gate length of the DMOS transistor is basically determined by diffusion coefficients by different ions and a diffusion started position, there is also a problem that the degree of the freedom in design of gate length is small.

SUMMARY OF THE INVENTION

The invention is made to solve the problems and a semiconductor device according to the invention is characterized in that, a gate electrode formed on a P-type well via a gate oxide film, a high-concentration N-type source layer and a high-concentration N-type drain layer respectively formed apart from the gate electrode and a low-concentration N-type source layer and a low-concentration N-type drain layer respectively formed so that they respectively surround the N-type source layer and the N-type drain layer and respectively parted by a P-type body layer formed under the gate electrode are provided.

Also, the semiconductor device according to the invention is characterized in that , a gate electrode formed on a first conductive type well via a gate oxide film , a high-concentration N-type source layer formed so that it is adjacent to one end of the gate electrode , a high-concentration second conductive -type drain layer formed apart from the other end of the gate electrode , a low-concentration first conductive type drain layer extended from under the gate electrode and

formed so that the low-concentration second conductive type drain layer surrounds the second conductive type drain layer and a second conductive type body layer formed between the second conductive type source layer under the gate electrode and the second conductive type drain layer are provided.

Preferably the step of forming the second conductive type body layer is formed by ion implantation.

According to the above feature, although channel length is determined as a one value in the convenient thermal procedure, since channel length can be determined more freely with respect to gate length according to designing the body layer, in comparison with the conventional method.

Further since the body layer of the present invention is formed only below the gate electrode, junction capacity can be reduced in comparison with the conventional body layer formed so as to cover the high concentration source layer.

Furthermore, high temperature thermal procedure for forming the body layer after forming the gate electrode is not required, hybrid integration with very small sized process can be realized.

Further, preferably p type layer for controlling a threshold voltage is formed on a surface portion (channel region) of the N type body layer is formed.

According to the above feature, a driving ability of p

channel DMOS transistor normally being inferior to n channel DMOS transistor can be improved.

According to the present invention, by forming impurity layer of each conduction type in each of the channel layers corresponding to the conduction type of the body layers, the driving capability of reverse conduction type of transistors formed on a substrate can be made uniform.

In the same conduction type of transistors which are different size, by forming impurity layer of conduction type in the channel layers of the body layers, the driving capability can be controlled.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 are sectional views showing a method of manufacturing a semiconductor device equivalent to an embodiment of the invention;

Figs. 2 are sectional views showing the method of manufacturing the semiconductor device equivalent to the embodiment of the invention;

Figs. 3 are sectional views showing the method of manufacturing the semiconductor device equivalent to the embodiment of the invention;

Figs. 4 are sectional views showing the method of manufacturing the semiconductor device equivalent to the embodiment of the invention;

Figs. 5 are sectional views showing the method of manufacturing the semiconductor device equivalent to the embodiment of the invention;

Figs. 6 are sectional views showing the method of manufacturing the semiconductor device equivalent to the embodiment of the invention;

Figs. 7 are sectional views showing the method of manufacturing the semiconductor device equivalent to the embodiment of the invention;

Figs. 8 are sectional views showing the method of manufacturing the semiconductor device equivalent to the embodiment of the invention;

Figs. 9 are sectional views showing the method of manufacturing the semiconductor device equivalent to the embodiment of the invention;

Figs. 10 are sectional views showing the method of manufacturing the semiconductor device equivalent to the embodiment of the invention;

Figs. 11 are sectional views showing the method of manufacturing the semiconductor device equivalent to the embodiment of the invention;

Figs. 12 are sectional views showing the method of manufacturing the semiconductor device equivalent to the another embodiment of the invention;

Fig. 13 is a sectional view showing a method of manufacturing a semiconductor device equivalent to the other embodiment of the invention; and

Fig. 14 is a sectional view showing a conventional type semiconductor device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to the drawings, an embodiment of a semiconductor device and its manufacturing method according to the invention will be described below.

A semiconductor device according to the invention shown in Fig. 10, that is, a driver for driving a liquid crystal is composed of an N-channel MOS transistor and a P-channel MOS transistor which are respectively a logic device of 3 V for example, an N-channel MOS transistor for a level shifter of 30 v for example, an N-channel MOS transistor of 30 V for example which has high resistance to voltage respectively in order from the left side in Fig. 10A, a P-channel MOS transistor of 30 V for example which has high resistance to voltage respectively, an N-channel DMOS transistor and a P-channel DMOS transistor respectively similarly in order from the left side in Fig. 10B.

A method of manufacturing various MOS transistors composing the driver for driving a liquid crystal will be described below.

First, as shown in Fig. 1, to define an area for composing

various MOS transistors, a P-type well (PW) 3 and an N-type well (NW) 5 are formed in a P-type semiconductor substrate (P-Sub) 1 for example.

That is, boron ions for example are implanted at the acceleration voltage of approximately 80 KeV under the implantation condition of 8 x $10^{12}/cm^2$ in a state that an area where the N-type well in the substrate 1 is formed is covered with a resist film not shown via a pad oxide film 2. Afterward, phosphorus ions for example are implanted at the acceleration voltage of approximately 80 KeV under the implantation condition of 9 x $10^{12}/cm^2$ in a state that the P-type well 3 is covered with a resist film 4 as shown in Figs. 1. Actually, the P-type well 3 and the N-type well 5 are formed by thermically diffusing each ion implanted as described above (for example, for four hours in the atmosphere of N_2 of 1150°C).

Next, as shown in Figs. 2, to separate every MOS transistor, a device separation film 8 of approximately 500nm is formed according to LOCOS method and a thick gate oxide film 9 of approximately 80nm for high resistance to voltage is formed on an active area except the device separation film 8 by thermal oxidation.

Next, a first low concentration N-type source and P-type drain layers (hereinafter called an LN layer 10 and an LP layer 11) are formed using a resist film as a mask. That is, first,

phosphorus ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 120 KeV under the implantation condition of 8 x $10^{12}/cm^2$ in a state that an area except an area where the LN layer is formed is covered with a resist film not shown so as to form the LN layer 10. Afterward, boron ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 120 KeV under the implantation condition of 8.5 x $10^{12}/cm^2$ in a state that an area except an area where the LP layer is formed is covered with a resist film (PR) so as to form the LP layer 11. Actually, each ion implanted as described above is thermically diffused after an annealing process (for example, for two hours in the atmosphere of N_2 of 1100°C) which is a postprocess to be the LN layer 10 and the LP layer 11.

Next, as shown in Figs. 3, a second-low concentration N-type source drain layers (hereinafter called an SLN layer13 SLP layer 14)are formed between the LN layers 10 using a resist film as a mask and a surface-low concentration P-type source drain layers (hereinafter called an SLP layer 14) is formed between the LP layers 11 using a resist film as a mask. That is, first, phosphorus ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 120 KeV under the implantation condition of

1.5 x $10^{12}/cm^2$ in a state that an area except an area where the SLN layer is formed is covered with a resist film not shown so as to form the SLN layer 13 which ranges to the LN layer 10. Afterward, boron difluoride ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 140 KeV under the implantation condition of 2.5 x $10^{12}/cm^2$ in a state that an area except an area where the SLP layer is formed is covered with a resist film (PR) so as to form the SLP layer 14 which ranges to the LP layer 11. The impurity concentration of to the LN layer 10 and the SLN layer 13 , or the LP layer 11 and the SLP layer 14 are set respectively substantially equal or one of them is higher then others.

Further, as shown in Figs. 4, high concentration N-type source and P-type drain layers (hereinafter called an N+ layer 15 and a P+ layer 16) are formed using a resist layer as a mask. That is, first, phosphorus ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 80 KeV under the implantation condition of 2 x $10^{15}/cm^2$ in a state that an area except an area where the N+ layer is formed is covered with a resist film not shown so as to form the N+ layer 15 which ranges to the LN layer 10. Afterward, boron difluoride ions for example are implanted into the superficial layer of the substrate at the acceleration

voltage of approximately 140 KeV under the implantation condition of 2 x $10^{15}/cm^2$ in a state that an area except an area where the P+ layer is formed is covered with a resist film (PR) so as to form the P+ layer 16.

Next, as shown in Figs. 5, a P-type layer 18 (equivalent to the P-type body layer in conventional type structure) and an N-type layer 19 (equivalent to the N-type body layer in conventional type structure) respectively separating the SLN layer 13 and the SLP layer 14 are formed by doping impurities respectively of the reverse conductive type in the center of the SLN layer 13 which ranges to the LN layer 10 and in the center of the SLP layer 14 which ranges to the LP layer 11 by ion implantation using a resist film as a mask. That is, first, boron difluoride ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 120 KeV under the implantation condition of 5 x $10^{12}/cm^2$ in a state that an area except an area where the P-type layer is formed is covered with a resist film not shown so as to form the P-type layer 18. Afterward, phosphorus ions for example are implanted into the superficial layer of the substrate at the acceleration voltage of approximately 190 KeV under the implantation condition of 5 x $10^{12}/cm^2$ in a state that an area except an area where the N-type layer is formed is covered with a resist film (PR) so as to form the N-type layer 19. The

order of steps related to the ion implantation process shown in Figs. 3 to 5 can be suitably varied.

Further, the second P-type well(SPW) 21 and a second N-type well (SNW)22 are formed in the substrate (the P-type well 3) in areas where micro N-channel and P-channel MOS transistors are formed respectively for normal resistance to voltage.

That is, boron ions are similarly implanted into the superficial layer of the substrate at the acceleration voltage of approximately 50 KeV under a second implantation condition of $2.6 \times 10^{12}/cm^2$ in a state that an area except an area where the P-type layer is formed is covered with a resist film not shown so as to form the second P-type well 21 after boron ions for example are implanted into the P-type well 3 at the acceleration voltage of approximately 190 KeV under a first implantation condition of $1.5 \times 10^{13}/cm^2$ using a resist film not shown having its opening on an area where the N-channel MOS transistor is formed for normal resistance to voltage as a mask. Also, phosphorus ions for example are implanted into the P-type well 3 at the acceleration voltage of approximately 380 KeV under the implantation condition of $1.5 \times 10^{13}/cm^2$ using a resist film (PR) having its opening on an area where the P-channel MOS transistor is formed for normal resistance to voltage as a mask so as to form the second N-type well 22. In case a generator of the acceleration voltage of approximately

380 KeV is not provided, a double charging method in which phosphorus ion is implanted at the acceleration voltage of 190 KeV under the implantation condition of $1.5 \times 10^{13}/cm^2$ an d then phosphorus ion is implanted at the acceleration voltage of 150 KeV under the implantation condition of $4.0 \times 10^{12}/cm^2$ may be also adopted.

Next, as shown in Figs. 7, after the gate oxide film 9 on the areas where the N-channel and P-channel MOS transistors are formed respectively for normal resistance to voltage and on an area where an N-channel MOS transistor for a level shifter is formed is removed, a gate oxide film having desired thickness is newly formed on the areas.

That is, first, a gate oxide film 24 of approximately 14nm (approximately 7nm at this stage, however, the thickness is increased when a gate oxide film for normal resistance to voltage described later is formed) is overall formed for the N-channel MOS transistor for the level shifter by thermal oxidation. Next, after the gate oxide film 24 of the N-channel MOS transistor for the level shifter formed on the areas where the N-channel and P-channel MOS transistors are formed respectively for normal resistance to voltage is removed, a thin gate oxide film 25 for normal resistance to voltage (of approximately 7nm) is formed in this area by thermal oxidation.

Next, as shown in Figs. 8, a polysilicon film of

approximately 100nm is overall formed and after $POCl_3$ is thermically diffused in the polysilicon film as a thermically diffused source and electricity is conducted in the polysilicon film, a tungsten silicide (WSi_x) film of approximately 100nm and further, an SiO_2 film of approximately 150nm are laminated on the polysilicon film, are patterned using a resist film not shown and gate electrodes 27A, 27B, 27C, 27D, 27E, 27F and 27G for each MOS transistor are formed. The SiO_2 film functions as a hard mask in patterning.

Next, as shown in Figs. 9, low concentration source/drain layers are formed for the N-channel and P-channel MOS transistors for normal resistance to voltage.

That is, first, phosphorus ions for example are implanted using a resist film not shown coating an area except areas where low concentration source/drain layers for an N-channel MOS transistor for normal resistance to voltage are formed as a mask at the acceleration voltage of approximately 20 KeV under the implantation condition of $6.2 \times 10^{13}/cm^2$ so as to form low concentration N-type source/drain layers 28. Also, boron difluoride ions for example are implanted using a resist film (PR) coating an area except areas where low concentration source/drain layers for a P-channel MOS transistor for normal resistance to voltage are formed as a mask at the acceleration voltage of approximately 20 KeV under the implantation

condition of 2 x $10^{13}/cm^2$ so as to form low concentration P-type source/drain layers 29.

Further, as shown in Figs. 10, a TEOS film 30 of approximately 250nm is overall formed by LPCVD so that the gate electrodes 27A, 27B, 27C, 27D, 27E, 27F and 27G are coated and is anisotropically etched using a resist film (PR) having an opening on the areas where the N-channel and P-channel MOS transistors for normal resistance to voltage are formed as a mask. Hereby, a side wall spacer film 30A is formed on both side walls of the gate electrodes 27A and 27B as shown in Figs. 10 and the TEOS film 30 is left in an area coated by the resist film (PR) as it is.

Figs. 11A and 11B are X1-X1, and X2-X2 sectional views for showing width directions of the gate electrodes 27F and 27G of N channel type DMOS transistor and P channel type DMOS transistor shown in Fig.10B. High concentration source/drain layers are formed for the N-channel and P-channel MOS transistors for normal resistance to voltage using the gate electrode 18A, the side wall spacer film 30A, the gate electrode 18B and the side wall spacer film 30A as a mask.

That is, arsenic ions for example are implanted using a resist film not shown coating an area except areas where high

concentration source/drain layers for an N-channel MOS transistor for normal resistance to voltage are formed as a mask at the acceleration voltage of approximately 100 KeV under the implantation condition of 5 x $10^{13}/cm^2$ so as to form high concentration N+-type source/drain layers 31. Also, boron difluoride ions for example are implanted using a resist film not shown coating an area except areas where high concentration source/drain layers for a P-channel MOS transistor for normal resistance to voltage are formed as a mask at the acceleration voltage of approximately 40 KeV under the implantation condition of 2 x $10^{15}/cm^2$ so as to form high concentration P+-type source/drain layers 32.

The N-channel MOS transistor and the P-channel MOS transistor respectively for normal resistance to voltage, the N-channel MOS transistor for the level shifter, the N-channel MOS transistor and the P-channel MOS transistor respectively for high resistance to voltage, the N-channel DMOS transistor and the P-channel DMOS transistor respectively composing the driver for driving a liquid crystal are completed by forming a metallic wiring layer kept in contact with each high concentration source/drain layer 15, 16, 31 and 32 after a layer insulating film of approximately 600nmcomposed of the TEOS film, a BPSG film and others is overall formed though the drawing is omitted.

Also, the source/drain layers structure is composed symmetrically regarding simplicity in the manufacturing process in the embodiment described above as important, however, the present invention is not limited to this and asymmetrical source/drain layers structure may be also adopted.

That is, a semiconductor device equivalent to another embodiment in this case is characterized in that to explain an N-channel DMOS transistor for an example, as shown in Fig.12A a gate electrode 27F formed on a P-type semiconductor substrate 1 for example via a gate oxide film 9, a high concentration N-type source layer 15A formed so that it is adjacent to one end of the gate electrode 27F, a high concentration N-type drain layer 15A formed apart from the other end of the gate electrode 27F, a low concentration N-type drain layer 10A extended from under the gate electrode 27F and formed so that the low concentration N-type drain layer surrounds the N-type drain layer 15A and a P-type body layer 18A under the gate electrode 27F formed between the N-type source layer 15A and the N-type drain layer 10A are provided as shown in Fig. 11.

As for its manufacturing method, after N-type impurities (for example, phosphorus ions) are implanted into a P-type well 3 for example and a low concentration N-type drain layer 10A is formed, N-type impurities (for example, arsenic ions) are implanted into the substrate 1, a high concentration N-type

source layer 15A is formed so that it is adjacent to one end of a gate electrode 27F and a high concentration N-type drain layer 15A is formed in a position apart from the other end of the gate electrode 27F. Next, P-type impurities (for example, boron ions) are implanted into the substrate 1 and a P-type body layer 18A is formed from under one end of the gate electrode 27F so that the P-type body layer is adjacent to the N-type source layer 15A. After a gate oxide film 9 is formed on the P-type well 3, the gate electrode 27F has only to be formed on the gate oxide film 9.

As described above, in the structure according to the invention, as the P-type body layer or the N-type body layer is formed only under the gate electrode in the N-channel DMOS transistor and the P-channel DMOS transistor, the quantity of junction can be reduced, compared with the conventional type structure where the high concentration source layer is wrapped by the P-type body layer or the N-type body layer.

Also, as in the structure described above, the P-type body layer or the N-type body layer is formed by ion implantation, microminiaturization is enabled, compared with a conventional type formed by diffusion.

Further, according to the manufacturing method described above, as high temperature heat treatment after the gate electrode for forming the body layer is formed when the DMOS

transistor is formed as in a conventional method is not required, compatibility with a microminiaturizing process is enabled.

Also, although channel length is determined as a one value in the convenient thermal procedure, in the method of manufacturing the DMOS transistor according to the invention, as the P-type body layer or the N-type body layer is formed after its own ion implantation process as described above, the degree of the freedom in design of gate length is increased, compared with the conventional method.

According to the invention, as the P-type body layer or the N-type body layer is formed only under the gate electrode in the MOS transistor having high resistance to voltage, the quantity of junction can be reduced, compared with the conventional type structure where the high concentration source layer is wrapped(surrounded) by the P-type body layer or the N-type body layer.

Also, as high temperature heat treatment after the gate electrode for forming the body layer is formed when the MOS transistor having high resistance to voltage is formed as in the conventional method is not required, compatibility with a microminiaturizing process is enabled, and various drivers for a display element (for example, a driver for displaying a liquid crystal) and a controller can be integrated into one chip.

Next, another embodiment of the present invention will

be explained referring to the Figs.12B, 13A,and 13B.

In the embodiment, it is characterized in that N type layer 31,31A and P type layer 32 for controlling threshold voltage are formed in a surface portion(channel region)of P type body layer 18,18A and N type body layer 19 of the N channel type DMOS transistor and the P type DMOS transistor. Explanation using drawing is omitted. P channel type DMOS transistor is as same as the N channel type DMOS transistor as shown in Figs.12A and 12B, except for conduction type.

According to the above DMOS transistor, by forming an impurity region which has an reverse conduction type to that of the body layer, threshold voltage can be lowered and the driving capability can be improved.

In the step of forming a body layer, using an ion implantation is preferable. But in another doping step not only ion implantation but also diffusing step from gas phase or solid phase can be used.Further in the DMOS transistors, by forming impurity layer of each conduction type in each of the channel layers corresponding to the conduction type of the body layers, the driving capability of reverse conduction type of transistors formed on a substrate can be made uniform.

In the same conduction type of DMOS transistors, by forming impurity layer of reverse conduction type in the channel layers of the body layers, the driving capability can be controlled.

According to the present invention, by forming a thin p type impurity region in a channel layer in each of the conduction type of body controlling the driving capability in the N channel DMOS transistor, the driving capability of the P-channel type DMOS transistor which is inferior to that of the N-channel type DMOS transistor can be improved. Further by controlling an impurity concentration of P type layer, the driving capability of the P-channel type DMOS transistor can be set same as that of the N-channel type DMOS transistor. Therefore it is not required to apply a high voltage in order to improve a switching characteristic of p channel type DMOS transistor. This invention has an advantage that low voltage driving can be performed.

WHAT IS CLAIMED IS:

1. A semiconductor device provided with high concentration source/drain layers of the reverse conductive type formed in a semiconductor layer of one conductive type, a gate electrode formed on a channel layer located between the source and drain layers, a body layer of one conductive type formed in the vicinity of the source layer and a low concentration drain layer of the reverse conductive type formed between the channel layer and the drain layer, wherein:

said body layer is formed only under said gate electrode.

2. A semiconductor device, according to claim 1, wherein the device comprises:

a gate electrode formed on a semiconductor layer of one conductive type via a gate oxide film;

a high concentration source layer of the reverse conductive type formed so that it is adjacent to one end of said gate electrode;

a high concentration drain layer of the reverse conductive type formed apart from the other end of said gate electrode;

a low concentration drain layer of the reverse conductive type extended from under said gate electrode and formed so that said low concentration drain layer of the reverse conductive type surrounds said drain layer of the reverse conductive type;

and

a body layer of one conductive type under said gate electrode formed between said source layer of the reverse conductive type and said drain layer of the reverse conductive type.

3. A semiconductor device, according to claim 1, wherein the device comprises:

a gate electrode formed on a semiconductor layer of one conductive type via a gate oxide film;

high concentration source/drain layers of the reverse conductive type formed apart from said gate electrode; and

low concentration source/drain layers of the reverse conductive type formed so that they respectively surround said source/drain layers of the reverse conductive type and parted by a body layer of one conductive type formed under said gate electrode.

4. A semiconductor device according to Claim 1, wherein:

said low concentration drain layer of the reverse conductive type or said low concentration source/drain layers of the reverse conductive type are formed so that they are shallow under said gate electrode and are deep under said high concentration drain layer of the reverse conductive type or said high concentration source/drain layers of the reverse

conductive type.

5. A semiconductor device, according to claim 1, wherein a reverse conductive type layer is formed in a surface portion of the body layer.

6. A method of manufacturing a semiconductor device provided with high concentration source/drain layers of the reverse conductive type formed in a semiconductor layer of one conductive type, a gate electrode formed on a channel layer located between the source and drain layers, a body layer of one conductive type formed in the vicinity of the source layer and a low concentration drain layer of the reverse conductive type formed between the channel layer and the drain layer, wherein the step of forming a body layer of one conductive type comprises a step of doping impurities of one conductive type into said semiconductor layer by ion implantation.

7. A method of manufacturing a semiconductor device provided with high concentration source/drain layers of the reverse conductive type formed in a semiconductor layer of one conductive type, a gate electrode formed on a channel layer located between the source and drain layers, a body layer of one conductive type formed in the vicinity of the source layer and a low concentration drain layer of the reverse conductive type formed between the channel layer and the drain layer , comprising the steps of :

doping impurities of the reverse conductive type into said semiconductor layer to form a low concentration drain layer of the reverse conductive type;

doping impurities of the reverse conductive type into said semiconductor layerto form a high concentration source layer of the reverse conductive type so that the source layer is adjacent to one end of said gate electrode and form a high concentration drain layer of the reverse conductive type in a position apart from the other end of said gate electrode;

doping impurities of one conductive type into said semiconductor layer to form a body layer of one conductive type extended from under one end of said gate electrode and formed so that the body layer is adjacent to said source layer of the reverse conductive type; and

forming a gate electrode on a gate oxide film after the gate oxide film is formed on said semiconductor layer.

8. A method of manufacturing a semiconductor device according to Claim 7, further comprising a step of doping an impurity for forming a reverse conduction type layer by ion implantation.

9. A method of manufacturing a semiconductor device according to Claim 7, wherein:

said low concentration drain layer of the reverse conductive type or said low concentration source/drain layers

of the reverse conductive type are formed so that they are shallow under said gate electrode and they are deep under said high concentration drain layer of the reverse conductive type or said high concentration source/drain layers of the reverse conductive type.

10. A method of manufacturing a semiconductor device, comprising the steps of:

doping impurities of the reverse conductive type into a semiconductor layer of one conductive type to form low concentration source/drain layers of the reverse conductive type;

doping impurities of the reverse conductive type into said semiconductor layer and forming a layer of the reverse conductive type which ranges to said source/drain layers of the reverse conductive type and is shallower than said source/drain layers of the reverse conductive type;

doping impurities of the reverse conductive type into said source/drain layers of the reverse conductive type to form high concentration source/drain layers of the reverse conductive type;

doping impurities of one conductive type into said layer of the reverse conductive type to form a body layer of one conductive type; and

forming a gate electrode on a gate oxide film so that the

gate electrode covers said body layer of one conductive type after the gate oxide film is formed on said substrate.

11. A method of manufacturing a semiconductor device according to Claim 10, further comprising a step of doping an impurity for forming a reverse conduction type layer by ion implantation after forming the body layer.

12. A method of manufacturing a semiconductor device, comprising the steps of:

doping impurities of the reverse conductive type into a semiconductor layer of one conductive type to forma low concentration layer of the reverse conductive type;

doping impurities of the reverse conductive type into said layer of the reverse conductive type to form high concentration source/drain layers of the reverse conductive type;

doping impurities of one conductive type into said layer of the reverse conductive type to form a body layer of one conductive type;

forming a first gate electrode for a first MOS transistor on a gate oxide film after the gate oxide film is formed on said substrate and forming a second gate electrode for a second MOS transistor on said body layer of one conductive type; and

forming source/drain layers of the reverse conductive type so that they are adjacent to said first gate electrode using

a resist film coating an area except are as where source/drain layers for said first MOS transistor are formed as a mask.

13. A method of manufacturing a semiconductor device according to Claim 12, further comprising a step of doping an impurity for forming a reverse conduction type layer by ion implantation.

14. A method of manufacturing a semiconductor device, comprising the steps of :

a doping impurities of the reverse conductive type into a semiconductor layer of one conductive type by ion implantation to form low concentration source/drain layers of the reverse conductive type;

doping impurities of the reverse conductive type into said semiconductor layer by ion implantation to form a layer of the reverse conductive type which ranges to said source/drain layers of the reverse conductive type and is shallower than said source/drain layers of the reverse conductive type;

doping impurities of the reverse conductive type into said source/drain layers of the reverse conductive type by ion implantation to form high concentration source/drain layers of the reverse conductive type;

doping impurities of one conductive type into said layer of the reverse conductive type by ion implantation to form a body layer of one conductive type;

forming a first gate electrode for a first MOS transistor on a gate oxide film after the gate oxide film is formed on said substrate to form a second gate electrode for a second MOS transistor on said body layer of one conductive type; and

forming source/drain layers of the reverse conductive type so that they are adjacent to said first gate electrode using a resist film coating an area except areas where the source/drain layers for said first MOS transistor are formed as a mask.

15. A method of manufacturing a semiconductor device according to Claim 14, further comprising a step of doping an impurity for forming a reverse conduction type layer by ion implantation.

16. A method of manufacturing a semiconductor device according to Claim 7, wherein said step of doping impurities of one conductive type into said semiconductor layer to form a body layer comprise a step of doping by ion implantation.

17. A method of manufacturing a semiconductor device according to Claim 10, wherein said step of doping impurities of one conductive type into said semiconductor layer to form a body layer comprise a step of doping by ion implantation.

18. A method of manufacturing a semiconductor device according to Claim 12, wherein said step of doping impurities of one conductive type into said semiconductor layer to form

a body layer comprise a step of doping by ion implantation.

19. A method of manufacturing a semiconductor device according to Claim 14, wherein said step of doping impurities of one conductive type into said semiconductor layer to form a body layer comprise a step of doping by ion implantation.

20. A method of manufacturing a semiconductor device according to Claim 12 , wherein:

said first MOS transistor is a micro MOS transistor; and

said second MOS transistor is a MOS transistor having high resistance to voltage.

21. A method of manufacturing a semiconductor device according to Claim 14 , wherein:

said first MOS transistor is a micro MOS transistor; and

said second MOS transistor is a MOS transistor having high resistance to voltage.

ABSTRACT

This invention is characterized in that, a gate electrode 27Fformed on a P-type well 3 via a gate oxide film 9, a high-concentration N-type source layer and a high-concentration N-type drain layer 15 respectively formed apart from the gate electrode and a low-concentration N-type source layer and a low-concentration N-type drain layer respectively formed so that they respectively surround the N-type source layer and the N-type drain layer 10 and respectively parted by a P-type body layer formed under the gate electrode 27F are provided.

Fig. 1 (a)

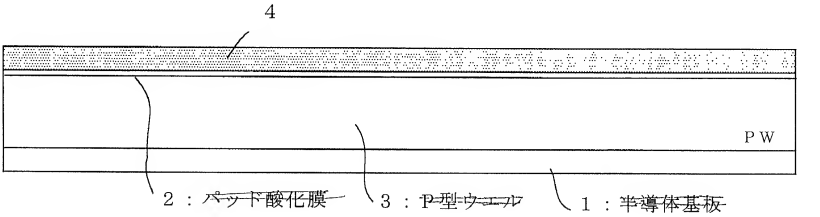


Fig. 1 (b)

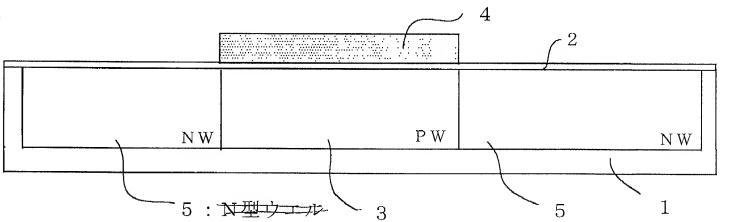


Fig.2 (a)

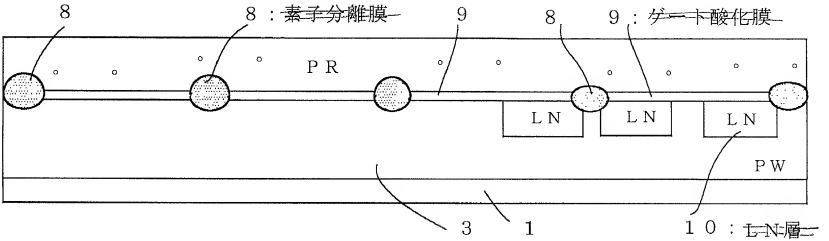
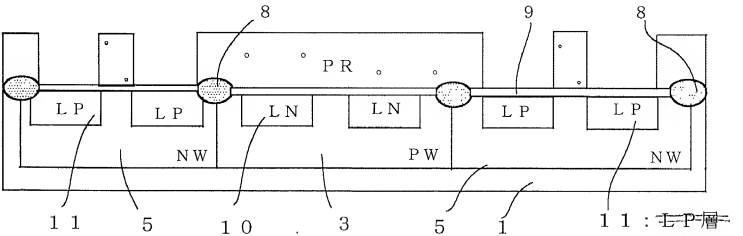

8
8：~~素子分離膜~~
9
8
9：~~ゲート酸化膜~~
PR
LN
LN
LN
PW
3
1
10：~~LN層~~

Fig.2 (b)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9
8
PR
LP
LP
LN
LN
LP
LP
NW
PW
NW
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5
10
3
5
1
11：~~LP層~~

Fig.3 (a)

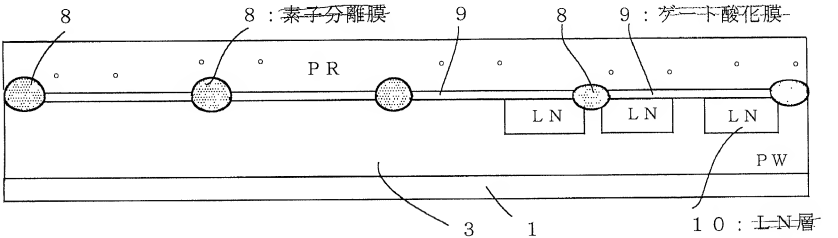
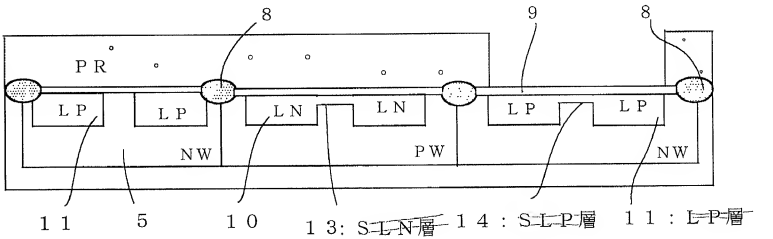

8
8：素子分離膜
9
8
9：ゲート酸化膜
PR
LN
LN
LN
PW
3
1
10：LN層

Fig.3 (b)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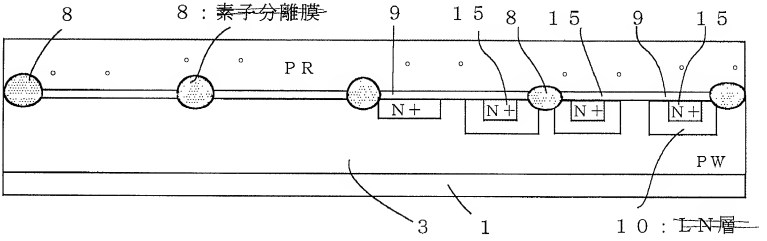
9
8
PR
LP
LP
LN
LN
LP
LP
NW
PW
NW
11
5
10
13: SLN層
14：SLP層
11：LP層

Fig.4(a)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15
8
15
9
15
PR
N+
N+
N+
N+
PW
3
1
10：L-N層

Fig.4(b)

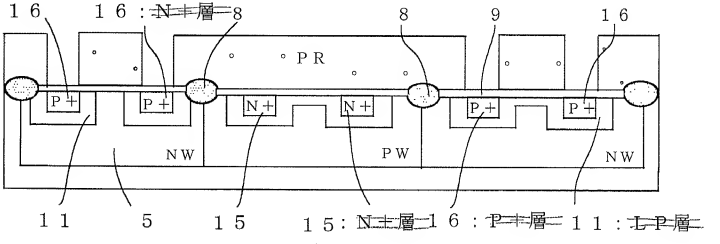

16
16：N+層
8
8
9
16
PR
P+
P+
N+
N+
P+
P+
NW
PW
NW
11
5
15
15：N+層
16：P+層
11：L-P層

Fig. 5 (a)

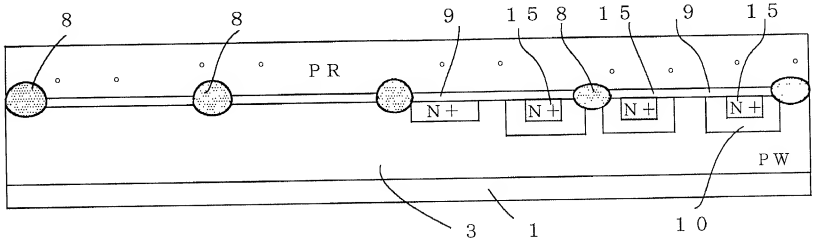

8
8
9
15
8
15
9
15
PR
N+
N+
N+
N+
PW
3
1
10

Fig. 5 (b)

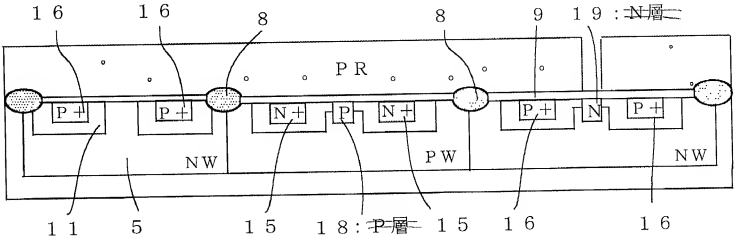

16
16
8
8
9
19：N層
PR
P+
P+
N+
P
N+
P+
N
P+
NW
PW
NW
11
5
15
18：P層
15
16
16

Fig.6 (a)

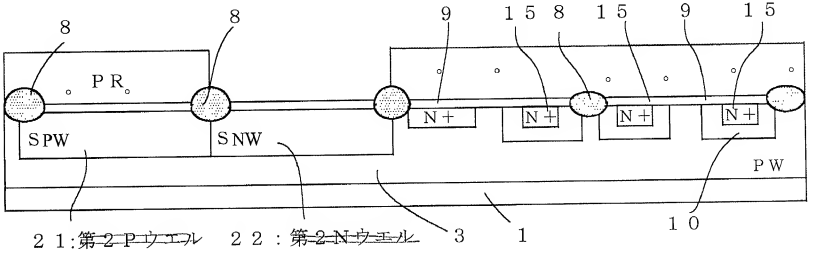


Fig.6 (b)

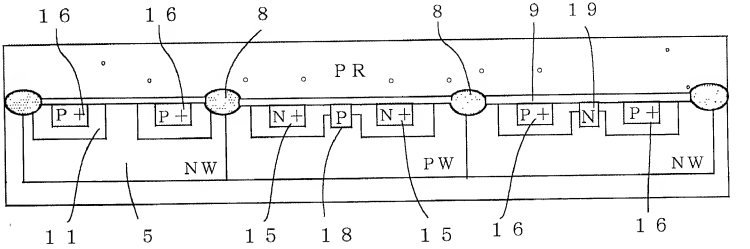


Fig.7 (a)

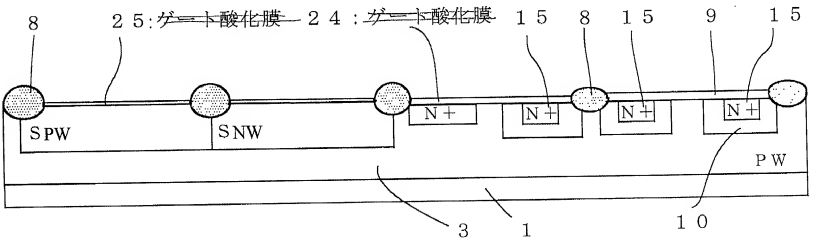
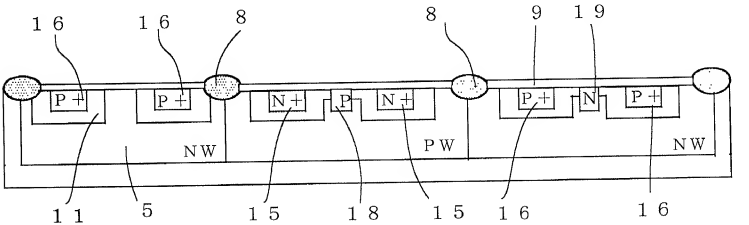

8
25:ゲート酸化膜
24:ゲート酸化膜
15
8
15
9
15
N+
N+
N+
N+
SPW
SNW
PW
3
1
10

Fig.7 (b)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16
8
8
9
19
P+
P+
N+
P
N+
P+
N
P+
NW
PW
NW
11
5
15
18
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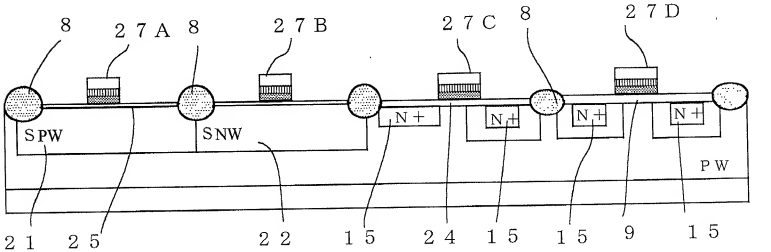
16
16

Fig. 8 (a)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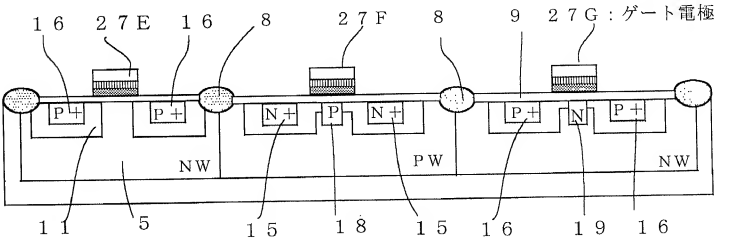
27A
8
27B
27C
8
27D
SPW
SNW
N+
N+
N+
N+
PW
21
25
22
15
24
15
15
9
15

Fig. 8 (b)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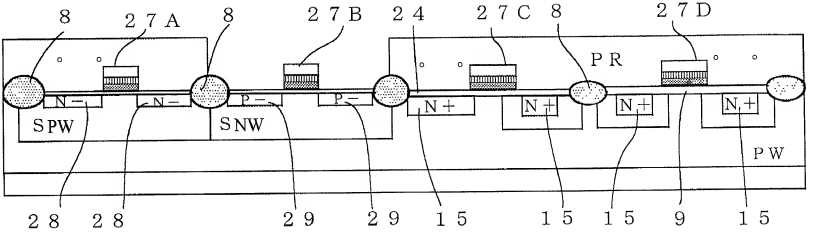
27E
16
8
27F
8
9
27G：ゲート電極
P+
P+
N+
P
N+
P+
N
P+
NW
PW
NW
11
5
15
18
15
16
19
16

Fig. 9 (a)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27A
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27B
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27C
8
27D
PR
N−
N−
P−
P−
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N+
N+
N+
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SNW
PW
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28
29
29
15
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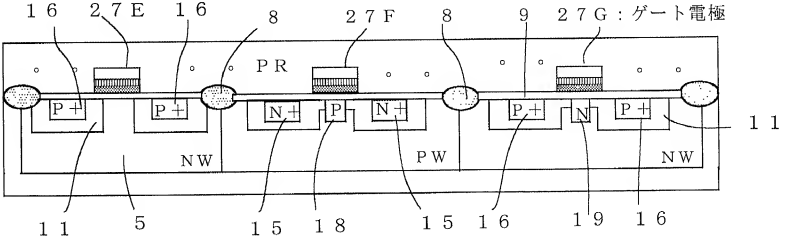
15

Fig. 9 (b)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27E
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P+
N+
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N+
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16

Fig.10 (a)

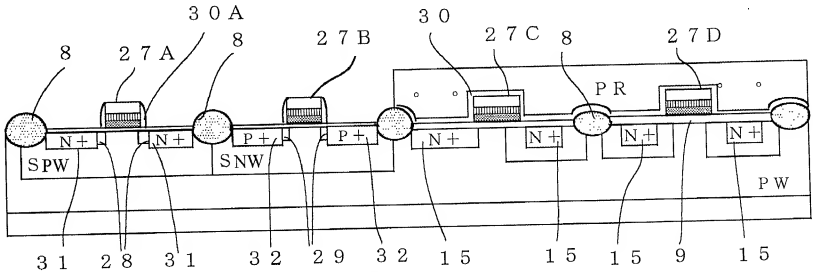


Fig.10 (b)

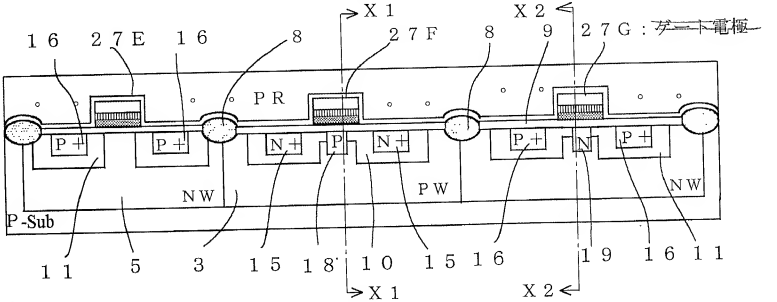


Fig. 11 (a)

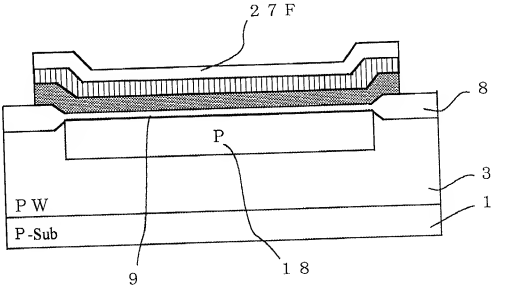


Fig. 11 (b)

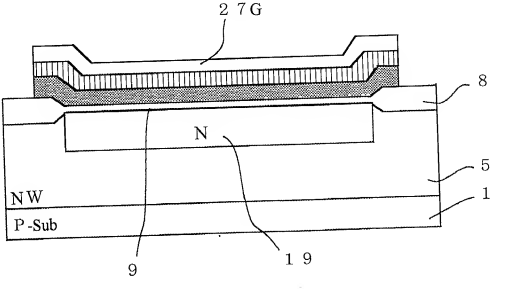


Fig.12 (a)

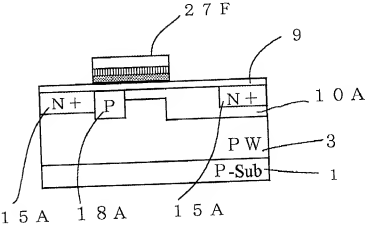


Fig.12 (b)

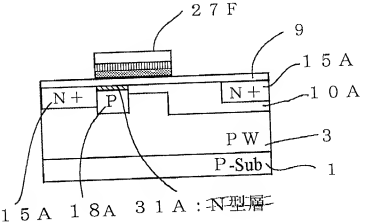


Fig. 13 (a)

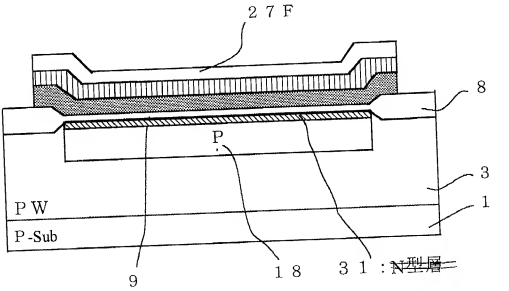


Fig. 13 (b)

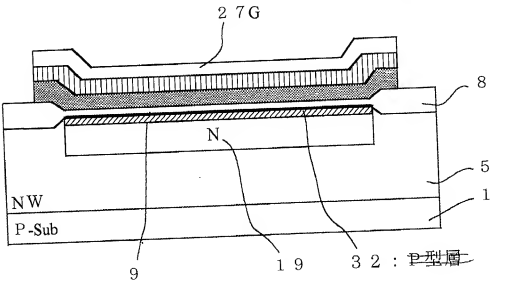
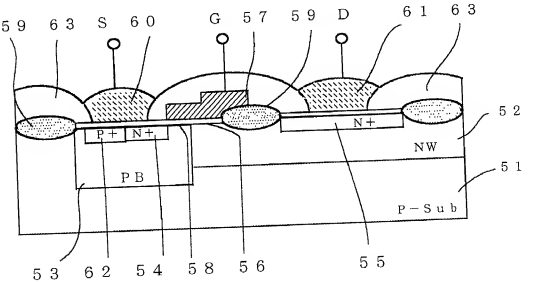


Fig. 14



Declaration and Power of Attorney for Patent Application
特許出願宣言書及び委任状

Japanese Language Declaration
日本語宣言書

下記の氏名の発明者として、私は下記の通り宣言します：

As a below named inventor, I hereby declare that:

私の住所、郵送先、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の氏名が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THEREOF

上記発明の明細書（下記の欄で×印がついていない場合は、本状に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ ___年___月___日に提出され、米国出願番号または特許協力条約国際出願番号を_____とし、（該当する場合）___年___月___日に訂正されました。

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable)

私は、特許請求範囲を含む上記補正による補正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendement referred to above.

私は、連邦規則法典第３７編第１条５６項に規定されるとおり、特許性の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Declaration and Power of Attorney for Patent Application
特許出願宣言書及び委任状

私は、米国法典第３５編１１９条 (a) - (d) 項又は３６５条(b) 項に基づき下記の、米国以外の国の少なくともーカ国を指定している同編３６５条 (a) 項に基づく特許協力条約国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願または特許協力条約国際出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority not claimed 優先権主張なし
P.Hei.11-309366	Japan	29/October/1999	☐
			☐

私は、第３５編米国法典１１９条 (e) 項に基づいて下記の米国特許予備出願の権利をここに主張いたします。

I hereby claim the benefits under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基づいて下記の米国特許出願の権利、又は米国を指定している特許協力条約国際出願３６５条 (c) に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項で規定された態様で先行する米国特許出願または特許協力条約国際出願に開示されていない限り、連邦規則法典第３７編１条５６項で定義されたその先行米国出願書提出日以降で国内または特許協力条約国際提出日までの期間中に入手し得た、特許性に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の表明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Declaration and Power of Attorney for Patent Application
特許出願宣言書及び委任状

委任先：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する代理人として、下記の者を指名いたします。*(代理人の氏名及び登録番号を明記のこと)*

POWER OF ATTORNEY: as named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

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